

REMARKS

In response to the Office Action mailed May 2, 2006, Applicants respectfully request reconsideration of the Application in view of the foregoing Amendments and the following Remarks. The claims as now presented are believed to be in allowable condition.

Claims 1, 4-6, 9-11, 14-17, 19, and 20 have been amended. Claims 1-20 remain in this application, of which claims 1 and 20 are independent claims.

Objection to Specification

The Title of the Present Application has been amended to overcome the Examiner's objection.

Objection to Claims

Claim 17 has been amended to overcome the Examiner's objection.

Rejection of Claims 1-20 under 35 U.S.C. §103(a)

Claims 1-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over "Mobile Ion-Induced Data Retention Failure in NOR Flash Memory Cells", IEEE Transactions on Device and Materials Reliability, Vol. 1, No. 2, June 2001 to Lee et al. (hereafter referred to as "Lee") in view of U.S. Patent No. 6,308,249 to Okazawa (hereafter referred to as "Okazawa"). Applicants respectfully traverse this rejection.

The rejection of claims 1 and 11 under 35 U.S.C. §103(a) as being unpatentable over Lee in view of Okazawa is not appropriate because claims 1 and 11 have been amended, and a prima facie case of obviousness cannot be established for such amended claims.

In giving an obviousness rejection, the Examiner bears the initial burden of factually supporting a prima facie conclusion of obviousness. (See, MPEP, §2142). To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be *some suggestion*

or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, *the prior art references* must teach or suggest *all the claim limitations*. (See, MPEP, §2142.) (Emphasis added.)

The rejection of amended claims 1 and 11 under 35 U.S.C. §103(a) as being unpatentable over Lee in view of Okazawa is not appropriate because *inter alia* these prior art references fail to teach or suggest all the claim limitations and because there is no motivation or suggestion in these references to combine or modify these references to the present invention.

Amended claims 1 and 11 recite determining an operating life of a memory device by applying stressing signals on a respective at least one cell of the memory device corresponding to each generated address during the cycling through of the addresses of the memory device, for a predetermined stress time period. In addition, amended claims 1 and 11 recite *minimizing charge gain failure* in the memory device after the predetermined stress time period with a transition of less than the predetermined number of bits for sequencing to each subsequent address during the cycling through of the addresses.

Support for such limitations is found at page 7, lines 25-31, page 8, lines 25-28, and page 15, lines 14-20 of the Present Application which states:

For any particular address, the word line of the row indicated by such an address has applied thereon the clock signal from the clock signal generator 164. The clock signal is a typical square wave clock signal with a frequency of 1 MHz for example and with an amplitude similar to the voltage VDS from the bit line voltage generator 190. Furthermore, the bit line of the column for each of the eight I/O's as specified by such an address has applied thereon the bit line voltage VDS that is about 6.5 Volts for example from the bit line voltage generator 190....

.... During such a stress time period of 168 hours, the clock signal from the clock signal generator 164 and the bit line voltage VDS from the voltage generator 170 are

applied on the eight flash memory cells of the array 152 as specified by the address bits....

.... In that case, no charge gain failure occurs because a bit transition occurs for only one bit in incrementing or decrementing to a subsequent address in the bit pattern for the address bits A'[20:0] in gray code sequence. Such address bits A'[20:0] in gray code sequence are applied to the burn-in board 174 in Fig. 9. Thus, because of such a small number of bit transitions for going to a subsequent address in cycling through each address of the flash memory device 160, no charge gain failure occurs with the HTOL test system 200 of Fig. 9.

Lee only discloses baking the memory device for 24 hours at 250° C for study of ion-induced data retention failure from non-optimized fabrication process parameters as stated at the first paragraph of Lee:

....The NOR-type cell has been widely investigated with respect to reliability including tunnel oxide integrity, interpoly dielectrics, and exterior contamination. All these nonoptimized process parameters cause charge variations on the floating gate....

As stated, Lee is directed to study of ion-induced data retention failure from fabrication failure. Thus, Lee just heats up the memory device 24 hours at 250° C to exaggerate the ion-induced effects from such fabrication failure, without any mention what-so-ever of applying stressing bias signals.

In contrast, the Present Invention is directed to characterizing the operating life of a memory device that is fabricated substantially properly by applying stressing bias signals during the stress time period.

Okazawa discloses accessing a memory device within a computer system using gray code address sequencing for minimizing power consumption. The Examiner states that the motivation to combine Lee and Okazawa is to minimize power consumption in the Present Application.

However, Applicants respectfully but strongly disagree with such motivation. Note that in a computer system, the memory device is accessed continuously by the main processor during

the 3-5 year life-time of a typical computer system. Thus, power conservation is important for such continual access in Okazawa.

In contrast, the Present Invention as recited in amended claims 1 and 11 is directed to testing of a memory device using a test system. Such testing occurs instantly in “one-shot” with the test system providing the power to the memory device. Thus, power conservation is not necessarily a motivation for such testing of the memory device.

In addition, please note in the test system 200 of FIG. 9 of the Present Application, including the binary to gray code converter 204 between the address generator 150 and the address signal driver 182 would just increase the number of components and thus would actually increase power consumption from the alternative scenario of not including the binary to gray code converter 204. Including such an additional component 204 would add cost and power consumption to the test system 200. Thus, one of ordinary skill in the art would not be motivated to add the additional component 204 to the test system 200 for conserving power.

Rather, the reason why Applicants use the binary to gray code converter 204 as an additional component in the test system 200 of FIG. 9 (despite the higher cost and higher power consumption) is that Applicants for the first time were surprised to find that charge gain failure after the stress time period is minimized and even eliminated in the memory device for HTOL testing. Experimentation by the Applicants that lead to such discovery of minimization and even elimination of charge gain failure is thoroughly described in reference to the Table of FIG. 12 in the Present Application.

Okazawa which uses the gray code sequence for typical accessing of a memory device in a computer system does not even remotely mention using the gray code sequence during testing

of the memory device for minimizing charge gain failure after the stress time period during HTOL testing.

Rather, Okazawa which is directed to typical accessing of a memory device by a main processor within a computer system is non-analogous art from the Present Invention as recited in amended claims 1 and 11 which are directed to testing to determine the operating life of a memory device.

Thus, Lee and/or Okazawa, either individually or in combination do not disclose, teach, or suggest cycling through addresses of a memory device in gray code sequence with application of stressing signals during the stress time period for minimizing charge gain failure after the stress time period.

In addition, the Examiner is respectfully directed to the MPEP at §2143 which states that the fact that the claimed invention is within the capabilities of one of ordinary skill in the art is not sufficient *by itself* to establish prima facie obviousness, and that the mere fact that references *can be* combined or modified does not render the resultant combination or modification obvious *unless the prior art also suggests the desirability of the combination or modification.*

If the Examiner disagrees, the Examiner is respectfully requested to point out *exactly where*, including *specific column(s), line number(s), and/or figure element(s)* in Lee and/or Okazawa, a suggestion or motivation may be found for combining such references to result in the Present Invention as recited in amended claims 1 and 11.

Accordingly, a prima facie conclusion of obviousness of claims 1 and 11 cannot be established because Lee and/or Okazawa fail to suggest or motivate all the claim limitations of

claims 1 and 11, and the rejection of claims 1 and 11 under 35 U.S.C. §103(a) should be withdrawn.

Claims 2-10, which depend from and further limit claim 1, are allowable for at least the same reasons that claim 1 is allowable as stated above.

Claims 12-20, which depend from and further limit claim 11, are allowable for at least the same reasons that claim 11 is allowable as stated above.

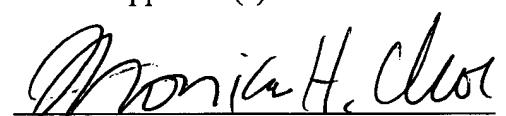
Conclusions

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. Please feel free to contact the undersigned should any questions arise with respect to this case that may be addressed by telephone.

Respectfully submitted,
for the Applicant(s)

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CERTIFICATE OF MAILING

The undersigned hereby certifies that the foregoing AMENDMENT AND RESPONSE is being deposited in the United States Postal Service, as first class mail, postage prepaid, in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 13th day of July, 2006.


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